I claim:

1. An apparatus, comprising:

a multiple-clock delay circuit to receive a reference clock signal and to provide multiple delayed output clock signals;

a selection circuit to receive an offset value and to receive the multiple delayed output clock signals, the selection circuit including an output circuit having an output load to output data timed with a first selected one of the multiple delayed output clock signals; and

a synchronization circuit coupled to the multiple-clock delay circuit and the selection circuit and having a load simulation circuit to simulate the output load, the synchronization circuit to receive the reference clock signal and the multiple delayed output clock signals.

2. The apparatus of claim 1, wherein:

the multiple-clock delay circuit includes a delay-locked loop circuit.

3. The apparatus of claim 1, wherein:

the synchronization circuit includes a first multiplexer to select a second selected one of the multiple delayed output clock signals to synchronize an intermediate clock signal with the reference signal.

4. The apparatus of claim 3, wherein:
the synchronization circuit includes a phase detector coupled to the multiplexer to detect a phase relationship between the reference clock signal and the intermediate clock signal.

5. The apparatus of claim 4, wherein:
the synchronization circuit includes an up/down counter coupled to the phase detector and the first multiplexer.

6. The apparatus of claim 1, wherein:
the selection circuit includes an adder circuit to add the first selection value to an offset value to produce a second selection value.

7. The apparatus of claim 6, wherein:
the selection circuit includes a second multiplexer coupled to the adder circuit to select a second one of the delayed output clock signals with the second selection value.

8. A system, comprising:
a processor;
a synchronous dynamic random access memory; and
a clock delay control circuit coupled to the processor and the memory, the clock delay control circuit including:
a multiple-clock delay circuit to receive a reference clock signal and to provide multiple delayed output clock signals;

a selection circuit to receive an offset value and to receive the multiple delayed output clock signals, the selection circuit including an output circuit having an output load to output data timed with a first selected one of the multiple delayed output clock signals; and

a synchronization circuit coupled to the multiple-clock delay circuit and the selection circuit and having a load simulation circuit to simulate the output load, the synchronization circuit to receive the reference clock signal and the multiple delayed output clock signals.

9. The system of claim 8, wherein:

the multiple-clock delay circuit includes a delay-locked loop circuit.

10. The system of claim 8, wherein:

the synchronization circuit includes a first multiplexer to select a second selected one of the multiple delayed output clock signals to synchronize an intermediate clock signal with the reference signal.

11. The system of claim 10, wherein:

the synchronization circuit includes a phase detector coupled to the multiplexer to detect a phase relationship between the reference clock signal and the intermediate clock signal.

12. The system of claim 11, wherein:
the synchronization circuit includes an up/down counter coupled to the phase detector and the first multiplexer.

13. The system of claim 8, wherein:
the selection circuit includes an adder circuit to add the first selection value to an offset value to produce a second selection value.

14. The system of claim 13, wherein:
the selection circuit includes a second multiplexer coupled to the adder circuit to select a second one of the delayed output clock signals with the second selection value.

15. A method, comprising:
providing multiple delayed clock signals;
producing an intermediate clock from an output simulation circuit that simulates at least one characteristic of an output circuit;
determining a selection value that selects one of the delayed clock signals to synchronize the intermediate clock with a reference clock; and
adding an offset value to the selection value to select another of the delayed clock signals to provide an output signal from the output circuit, a phase of the output signal being delayed from the intermediate clock by an amount specified by the offset value.

16. The method of claim 15, wherein:

determining a selection value includes using a phase detector to determine a phase relationship between the intermediate clock and the reference clock.

17. The method of claim 15, wherein:

determining a selection value includes using an up/down counter to select said one of the delayed clock signals.

18. The method of claim 15, wherein:

said at least one characteristic includes a signal delay in the output circuit.

19. The method of claim 15, wherein:

said at least one characteristic includes an output load on the output circuit.

20. The method of claim 15, wherein:

providing multiple delayed clock signals includes providing clock signals with phase delays spanning a single cycle of the reference clock.